IFW 2823

Attorney's Docket No.: P8123 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
	)	
Brian Doyle	)	
	)	
U.S. Serial No: 09/516,653	)	Examiner: Kebede, Brook
	)	
Filed: March 1, 2000	)	Art Unit: 2823
	)	
For: QUANTUM WIR GATE DEVICE AND METHOD OF MAKING SAME	)	

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION TO REQUEST WITHDRAWAL OF HOLDING OF ABANDONMENT

Dear Sir:

This is in response to the Office Communication mailed May 27, 2004. The Examiner had sent a Notice of Abandonment on Form PTO-1432 in view of Applicant's failure to timely file a proper reply to the Office Action mailed November 6, 2003.

FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to MAIL STOP _____
COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450
U.S. Patent and Trademark Office, Washington, D.C. 20231 on June 8, 2004.
Date of Deposit

Teresa Mattox
Name of Person Mailing Correspondence

Teresa Mattox
Signature

June 8, 2004
Date

Applicant believes that the USPTO did in fact receive a properly filed reply to the subject case. Pursuant to 37 C.F.R. §1.181 and MPEP §711.03 (c), a petition to withdraw a holding of abandonment may be submitted within 2 months of the Notice of Abandonment and no fee is required.

Accordingly, Applicant herewith submits the following statement of the facts involved and the action requested. On February 3, 2004 an Amendment and Response to the Office Action mailed November 6, 2003 was timely filed. Applicant received a return postcard with a stamp by OIPE of the USPTO dated February 5, 2004. Per conversation with Examiner Brook Kebede on June 3, 2004, he instructed that filing a Petition to Withdraw Abandonment of the application is required. As such, Applicant respectfully requests the Examiner to withdraw the holding of abandonment and enter the reply.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 6/8, 2004

Michael A. Bernadicou
Reg. No. 35,934

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

W/

Serial/Patent No.: 09/516,653 Filing/Issue Date: March 1, 2000
Client: Intel Corporation
Title: QUANTUM WIR GATE DEVICE AND METHOD OF MAKING SAME

BSTZ File No.: 042390P8123 Atty/Secty Initials: MAB/CMW/te
Date Mailed: February 3, 2004 Docket Due Date: March 6, 2004

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

- [X] Amendment/Response (15 pgs.)
- [ ] Appeal Brief (____ pgs.) (in triplicate)
- [ ] Application - Utility (____ pgs., with cover and abstract)
- [ ] Application - Rule 1.53(b) Continuation (____ pgs.)
- [ ] Application - Rule 1.53(b) Divisional (____ pgs.)
- [ ] Application - Rule 1.53(b) CIP (____ pgs.)
- [ ] Application - Rule 1.53(d) CPA Transmittal (____ pgs.)
- [ ] Application - Design (____ pgs.)
- [ ] Application - PCT (____ pgs.)
- [ ] Application - Provisional (____ pgs.)
- [ ] Assignment and Cover Sheet
- [X] Certificate of Mailing
- [ ] Declaration & POA (____ pgs.)
- [ ] Disclosure Docs & Orig & Copy of Inventor's Signed Letter (____ pgs.)
- [ ] Drawings: ____ # of sheets includes ____ figures
- [ ] Express Mail No.: _____ [ ] Check No. _____
- [ ] _____ Month(s) Extension of Time Amt: _____
- [ ] Information Disclosure Statement & PTO-1449 (__ pgs.) [ ] Check No. _____
- [ ] Issue Fee Transmittal Amt: _____
- [ ] Notice of Appeal
- [ ] Petition for Extension of Time
- [ ] Petition for _____
- [X] Postcard
- [ ] Power of Attorney (____ pgs.)
- [ ] Preliminary Amendment (____ pgs.)
- [ ] Reply Brief (____ pgs.)
- [ ] Response to Notice of Missing Parts
- [ ] Small Entity Declaration for Indep. Inventor/Small Business
- [ ] Transmittal Letter, in duplicate
- [ ] Fee Transmittal, in duplicate

- [X] Other: Amendment Transmittal (in duplicate)

Serial/Patent No.: 09/516,653 Filing/Issue Date: March 1, 2000
Client: Intel Corporation
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- [ ] Assignment and Cover Sheet
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- [ ] Drawings: ____ # of sheets includes ____ figures
- [ ] Express Mail No.: _____ [ ] Check No. _____
- [ ] _____ Month(s) Extension of Time Amt: _____
- [ ] Information Disclosure Statement & PTO-1449 (__ pgs.) [ ] Check No. _____
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- [ ] Petition for _____
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- [ ] Reply Brief (____ pgs.)
- [ ] Response to Notice of Missing Parts
- [ ] Small Entity Declaration for Indep. Inventor/Small Business
- [ ] Transmittal Letter, in duplicate
- [ ] Fee Transmittal, in duplicate

- [x] Other: Amendment Transmittal (in duplicate)

AMENDMENT TRANSMITTAL **PATENT**

Application No.: 09/516,653
Filing Date: March 1, 2000
First Named Inventor Brian Doyle
Examiner's Name: Berezny, Neal
Art Unit: 2823
Attorney Docket No.: 042390P8123

____ An Amendment After Final Action (37 CFR 1.116) is attached and applicant(s) request expedited action.
__X__ Charge any fee not covered by any check submitted to Deposit Account No. 02-2666.
__X__ Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 CFR 1.16 and 1.17, for any concurrent or future reply to Deposit Account No. 02-2666.
____ Applicant(s) claim small entity status (37 CFR 1.27).

ATTACHMENTS

____ Preliminary Amendment
__X__ Amendment/Response with respect to Office Action
____ Amendment/Response After Final Action (37 CFR 1.116) (reminder: consider filing a Notice of Appeal)
____ Notice of Appeal
____ RCE (Request for Continued Examination)
____ Supplemental Declaration
____ Terminal Disclaimer (reminder: if executed by an attorney, the attorney must be properly of record)
____ Information Disclosure Statement (IDS)
____ Copies of IDS citations
____ Petition for Extension of Time
____ Fee Transmittal Document (that includes a fee calculation based on the type and number of claims)
____ Cross-Reference to Related Application(s)
____ Certified Copy of Priority Document
____ Other:
____ Other:
____ Check(s)
__X__ Postcard (Return Receipt)

SUBMITTED BY:

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CERTIFICATE OF MAILING BY FIRST CLASS MAIL (if applicable)

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Date of Deposit
Teresa Edwards
Name of Person Mailing Correspondence
Teresa Edwards
Signature
February 3, 2004
Date

(10/14/03)

Send to: COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, Virginia 22313-1450

Attorney Docket No. **42390.P8123** Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Brian Doyle

Serial No. 09/516,653

Filed: March 1, 2000

For: QUANTUM WIRE GATE DEVICE AND METHOD OF MAKING SAME

EXAMINER: BEREZNY, NEAL

ART UNIT: 2823

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed November 6, 2003, Applicant respectfully requests the Examiner to enter the following amendments and consider the following remarks.

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On February 3 2004
Date of Deposit

Teresa Edwards
Name of Person Mailing Correspondence

Teresa Edwards
Signature

February 3 2004
Date

IN THE CLAIMS

Please amend claims 1, 22, 49, and 50.

Please cancel claims 11, 13, 15, 23, and 48.

Please add claims 51-61.

1. (Currently Amended) A method of forming a device comprising:

patterning a first oxide upon a substrate;

forming a first nitride spacer mask upon the first oxide;

forming a first oxide spacer mask upon the first nitride spacer mask;

forming a second nitride spacer mask upon the first oxide spacer mask;

forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask, wherein adjacent channels are spaced apart by a trench that is at least as wide as each of the channels, and wherein a doping region is disposed in the substrate beneath the trench that resists electrical communication between adjacent spaced-apart channels; and

forming a gate layer over the plurality of channels, wherein each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein.

2. (Original) The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer.

3. (Original) The method according to claim 1, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer.

4. (Original) The method according to claim 1, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask; and

performing a reactive ion etch upon the second nitride layer.

5. (Original) The method according to claim 1, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing a gate etch with the second nitride spacer masks.

6. (Original) The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask; and

performing a reactive ion etch upon the second nitride layer, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing a gate etch with the second nitride spacer masks, and further comprising:

forming a gate oxide upon the plurality of channels.

7. (Original) The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 300 nm.

8. (Original) The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 320 nm.

9. (Original) The method according to claim 1, wherein the substrate is made by providing a silicon on insulator substrate, and wherein the plurality of channels comprises monocrystalline silicon channels.

10. (Original) The method according to claim 1, wherein the substrate comprises monocrystalline silicon, and wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels.

11. (Canceled)

12. (Original) The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein the trench is filled with a dielectric, and wherein the plurality of channels comprises a plurality of single-gate quantum wire field effect transistors.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Previously Presented) A method of forming a device comprising:

patterning a first oxide layer having a first width upon a substrate;

forming a first nitride layer upon the first oxide layer and the substrate, wherein the first nitride layer has a first thickness that is less than the first width;

forming a first nitride spacer mask from the first nitride layer, wherein the first nitride spacer mask has a width about equal to the first nitride layer thickness;

forming a second oxide layer upon the first nitride spacer mask, wherein the second oxide layer has a second thickness that is less than the width of the first nitride spacer mask;

forming a first oxide spacer mask from the second oxide layer, wherein the first oxide spacer mask has a width about equal to the second oxide layer thickness;

forming a second nitride layer upon the first oxide spacer mask, wherein the second nitride layer has a thickness that is less than the width of the first oxide spacer mask;

forming a second nitride spacer mask from the second nitride layer;

removing the first oxide spacer mask;

performing an etch over the second nitride spacer mask to form at least one semiconductor channel having a channel width and a length, wherein the mean free electron path therein is larger than the channel width;

forming a dielectric layer upon the channel length; and

forming a gate layer over the channel.

17. (Previously Presented) The method according to claim 16, wherein the first oxide has a pitch of about three times the first width.

18. (Original) The method according to claim 16, wherein each performing a spacer etch comprises performing a reactive ion etch.

19. (Previously Presented) A method, comprising:

forming a pattern of oxide structures upon a silicon layer, the oxide structures having a first width, the silicon layer overlying an insulator layer, and the insulator layer overlying a silicon substrate;

forming a first nitride spacer mask upon the first oxide structures;

forming a first oxide spacer mask upon the first nitride spacer mask;

forming a second nitride spacer mask upon the first oxide spacer mask; and

performing an etch over the second nitride spacer mask to form a silicon on oxide (SOI) structure including a plurality of quantum wires formed from the silicon layer that are aligned to the second nitride spacer mask, the quantum wires being narrower than the mean free path of semiconductive electron flow therein.

20. (Previously Presented) The method according to claim 19, wherein the first width of the oxide structures is approximately between 50nm to 200nm and the quantum wires have a second width that is about one-tenth the first width.

21. (Previously Presented) The method according to claim 19, further comprising:

forming an oxide upon the plurality of quantum wires;

forming a gate layer over the oxide; and

forming a contact that connects with the plurality of channels, wherein the contact has a characteristic third width from about 2 times the first width to about 10 times the first width.

22. (Currently amended) A method of forming a device comprising:

patterning a first oxide upon a substrate, wherein the first oxide has a characteristic width of X and a characteristic pitch selected from about 3X and about 3.2X;

forming a first nitride layer upon the first oxide, wherein the first nitride layer has a characteristic thickness of about one half X;

performing a spacer etch upon the first nitride layer and removing the first oxide to form a patterned first nitride spacer mask;

forming an oxide layer upon the patterned first nitride spacer mask, wherein the oxide layer has a characteristic thickness of about one fourth X;

performing a spacer etch upon the oxide layer and removing the patterned first nitride spacer mask to form a patterned first oxide spacer mask;

forming a second nitride layer upon the patterned first oxide spacer mask, wherein the second nitride layer has a characteristic thickness of about one-tenth X; ~~and~~

performing a spacer etch upon the second nitride layer and removing the first oxide spacer mask to form a patterned second nitride spacer mask; and

performing an etch over the patterned second nitride spacer mask to form at least one semiconductor channel wherein the mean free electron path therein is larger than about one-tenth X.

23. (Cancelled)

24. (Original) The method according to claim 22, wherein X is in a range from about 20 nm to about 200 nm.

25. (Original) The method according to claim 22, wherein each performing a spacer etch comprises performing an reactive ion etch.

26. (Previously Presented) The method according to claim 19, wherein the oxide structures further comprise a characteristic pitch of between about 3 to about 3.2 times the first width.

27. (Canceled)

28. (Canceled)

39. (Previously Presented) A method of forming a structure comprising:

forming a plurality of semiconductive channels, each of the plurality of semiconductive channels comprising a channel length and a channel width, the plurality of semiconductive channels being formed by forming a first nitride spacer mask on an semiconductive layer, forming a first oxide spacer mask upon the first nitride mask, forming a second nitride spacer mask upon the first oxide spacer mask, and etching the plurality of semiconductive channels into the semiconductive layer in alignment with the second nitride spacer mask;

forming a dielectric layer upon the semiconductive channel length;

forming a source at a first terminal end of the plurality of semiconductive channels;

forming a second terminal end of the plurality of semiconductive channels;

forming a gate layer over the dielectric layer, wherein electron flow in the plurality of semiconductive channels has a mean free path that is greater than the semiconductive channel width, and wherein a first semiconductive channel of the

plurality of semiconductive channels is spaced apart from a second semiconductive channel of the plurality of semiconductive channels by a trench that is less than about five times the semiconductive channel width.

40. (Previously Presented) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric.

41. (Previously Presented) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming a self-aligned doping region in the monocrystalline silicon beneath the trench.

42. (Previously Presented) The method according to claim 39, wherein the semiconductive channel width is formed in a range from less than or equal to about 5 nm to about 30 nm.

43. (Previously Presented) The method according to claim 39, further comprising:

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels upon a contact landing pad.

44. (Previously Presented) The device according to claim 39, further comprising:

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

45. (Previously Presented) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench.

46. (Previously Presented) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench; and

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact ahs a characteristic width in a range from about 200 nm to about 1,000 nm.

47. (Previously Presented) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric, wherein the semiconductive channel width is formed in a range from less than or equal to about 5 nm to about 30 nm and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench; and

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

48. (Cancelled)

49. (Currently Amended) The method of claim ~~48~~ 50, wherein the first material is a silicon material, the second material is a nitride material, and the third material is an oxide material.

50. (Currently Amended) ~~The~~ A method ~~of claim 48, further~~ comprising:

forming a plurality of semiconductive channels into a first material, each of the plurality of semiconductive channels comprising a channel width having a mean free path smaller than electron flow, the plurality of semiconductive channels being formed by forming at least two spacer masks, the at least two spacer masks comprising second and third materials that can be etched with an etch chemistry selective to each other and also selective to the first material;

forming the first spacer masks on the first material, each of the first spacer masks having a first width;

forming the second spacer masks along the sidewalls of the first spacer masks, each of the second spacer masks having a second width smaller than the first width of each of the first spacer masks;

etching the first spacer masks with an etch chemistry that entirely removes the first spacer masks but that does not etch the first material or the third material;

forming third spacer masks along the sidewalls of the second spacer masks, the third spacer masks also comprising the second material, each of the third spacer masks having a third width smaller than the second width of each of the second spacer masks, the third width being smaller than a mean free path of electron flow;

etching the second spacer masks with an etch chemistry that entirely removes the second spacer masks but that does not etch the first material or the third material; and

etching the first material in alignment with the sidewalls of the third spacer masks to form the plurality of semiconductive channels beneath the third spacer masks.

51. (New) A method comprising:

forming a plurality of quantum wires in a substrate, wherein each of the plurality of quantum wires is narrower than the mean free path of semiconductive electron flow therein;

forming a spacer mask over each of the plurality of quantum wires; and

forming a gate layer over the plurality of quantum wires, wherein the spacer mask is formed between the quantum wire and the gate layer.

52. (New) The method of claim 51, wherein the substrate is made by providing a silicon on insulator substrate, wherein the plurality of quantum wires comprises monocrystalline silicon channels, and wherein the plurality of quantum wires is spaced apart by a trench that is at least as wide as each of the channels.

53. (New) The method of claim 51, wherein the substrate comprises monocrystalline silicon, and wherein the plurality of quantum wires is spaced apart by a trench that is at least as wide as each of the channels.

54. (New) The method of claim 52, further comprising filling the trench with a dielectric.

55. (New) The method of claim 54, wherein the plurality of quantum wires comprises a plurality of double-gate quantum wire field effect transistors.

56. (New) A method comprising:

forming a plurality of quantum wires in a substrate, wherein each of the plurality of quantum wires is narrower than the mean free path of semiconductive electron flow therein and wherein a trench is formed between adjacent quantum wires;

disposing a doping region in the substrate beneath each trench to resist electrical communication between adjacent quantum wires; and

forming a gate layer over the plurality of quantum wires, wherein the spacer mask is formed between the quantum wire and the gate layer.

57. (New) The method of claim 56, wherein the substrate is made by providing a silicon on insulator substrate, wherein the plurality of quantum wires comprises monocrystalline silicon channels, and wherein the trench is at least as wide as each of the channels.

58. (New) The method of claim 56, wherein the substrate comprises monocrystalline silicon, and wherein the trench is at least as wide as each of the channels.

59. (New) The method of claim 56, further comprising filling the trench with a dielectric.

60. (New) The method of claim 59, wherein the plurality of quantum wires comprises a plurality of double-gate quantum wire field effect transistors.

61. (New) The method of claim 59, wherein the plurality of quantum wires comprises a plurality of triple-gate quantum wire field effect transistors.

REMARKS

Applicants have amended claims 1, 22, 49, and 50. Applicants have canceled claims 11, 13, 15, 23, and 48. Applicants have added claims 51-61. No new matter has been added by this amendment.

Claim Rejections - 35 U.S.C. § 112

The Examiner has rejected claims 22, 24, and 25 under 35 U.S.C. §112. Applicant has amended independent claim 22 so as to overcome the Examiner's rejection of these claims.

Claim Rejections – 35 U.S.C. § 102

The Examiner has rejected claims 1, 5, 10, 48, and 49 under 35 U.S.C. 102(e) as being anticipated by Doyle (U.S. Patent No. 6,063,688).

Applicant has amended claim 1 to include the limitation of canceled claim 11, which the Examiner noted would be allowable if rewritten with all of the limitations of the base claim and any intervening claims. Applicant respectfully submits that this amendment places claim 1 in condition for allowance. Claims 5 and 10 are dependent upon independent claim 1. Thus for at least the reasons describe above, Applicant respectfully submits that Doyle does not anticipate all elements of claims 5 and 10.

Claim 48 has been cancelled. Claim 49 has been amended to be made dependent upon independent claim 50. Applicant respectfully submits that this amendment places claim 49 in condition for allowance.

Claim Rejections: 35 U.S.C. § 103 – Statement of Common Ownership Under 35 U.S.C. §103(c)

The Examiner has rejected claims 2-4, 6-9, 12, 16-26, 39-40, 42-44, and 50 under 35 U.S.C. §103(a) as being unpatentable over Doyle (U.S. Patent No. 6,063,688).

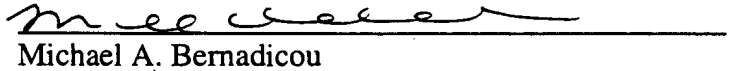
Applicants respectfully submit that under 35 U.S.C. §103(c), both the present application (Serial No. 09/516,653) and Doyle were, at the time the present invention was made, owned by, or subject to an obligation of assignment to Intel Corporation. Therefore, Doyle may not be used in a 35 U.S.C. §103 rejection against the claims of the present application, and qualifies as prior art only under 35 U.S.C. §102(e). (MPEP 706.02(l)(2))

Applicants respectfully submit the present application is in condition for allowance. Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 2/3/04



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